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Ultrahigh-mobility semiconducting epitaxial graphene on silicon carbide

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Semiconducting graphene plays an important part in graphene nanoelectronics because of the lack of an intrinsic bandgap in graphene[1]. In the past two decades, attempts to modify the bandgap either by quantum confinement or by chemical functionalization failed to produce viable semiconducting graphene. Here we demonstrate that semiconducting epigraphene (SEG) on single-crystal silicon carbide substrates has a band gap of 0.6 eV and room temperature mobilities exceeding 5,000 $cm^2 V^{-1} s^{-1}$, which is 10 times larger than that of silicon and 20 times larger than that of the other two-dimensional semiconductors. It is well known that when silicon evaporates from silicon carbide crystal surfaces, the carbon-rich surface crystallizes to produce graphene multilayers[2]. The first graphitic layer to form on the silicon-terminated face of SiC is an insulating epigraphene layer that is partially covalently bonded to the SiC surface[3]. Spectroscopic measurements of this buffer layer[4] demonstrated semiconducting signatures[4], but the mobilities of this layer were limited because of disorder[5]. Here we demonstrate a quasi-equilibrium annealing method that produces SEG (that is, a well-ordered buffer layer) on macroscopic atomically flat terraces. The SEG lattice is aligned with the SiC substrate. It is chemically, mechanically and thermally robust and can be patterned and seamlessly connected to semimetallic epigraphene using conventional semiconductor fabrication techniques. These essential properties make SEG suitable for nanoelectronics.

The graphene revolution was originally driven by the search for electronic materials that could outperform silicon[6]. Graphene, which is intrinsically a semimetal (that is, a gapless semiconductor), was considered to be a probable candidate[7,8] following predictions that, owing to quantum confinement, graphene nanoribbons can be semiconductors[9,10]. However, efforts to produce high-quality semiconducting ribbons were not successful[11]. Therefore, research focused on altering the electronic structure of graphene chemically, but efforts failed to produce a viable semiconductor[12]. After this, interest shifted away from graphene, towards other two-dimensional (2D) materials that are intrinsically semiconducting[1,13]. Here we show that well-annealed epigraphene on a specific silicon carbide crystal face is a 2D semiconductor with very high mobility.

Epigraphene is graphene that spontaneously forms on silicon carbide crystals when silicon sublimates from the surface at high temperatures resulting in a carbon-rich surface that recrystallizes into graphene[2,3]. Epigraphene on the silicon-terminated face of h-SiC has been the focus of much research[2,3]. The first graphitic layer to grow on this surface (the buffer layer), also has the graphene lattice structure, but it is partially covalently bonded to the SiC. The lattice of this structure is rotated by 30° with respect to the SiC lattice to produce a quasi-periodic $SiC_{6\times6}$ superlattice with a lattice constant of 1.85 nm, and it has an energy gap at the Fermi level[14,15], but it is disordered.

Angle-resolved photoelectron spectroscopy showed that the buffer layer produced in a confinement-controlled sublimation furnace[16] is better ordered[4] and is a potentially viable semiconductor[4,14,17,18]. However, the mobility μ of the buffer layer was found to be only $\mu = 1\ cm^2 V^{-1} s^{-1}$ (ref. 5) (Supplementary Information), which is small compared with that of other 2D semiconductors that have room temperature mobilities up to about 300 $cm^2 V^{-1} s^{-1}$ (refs. 1,19).

X-ray reflection studies of the buffer layer show that the underlying SiC surface is markedly depleted of silicon[20,21]. This can be expected because the buffer layer is produced by the thermal depletion of silicon at high temperatures. The buffer layer is found to have a perfect graphene structure; however, the bonding to the substrate is disordered resulting in small mobilities[5,22].

Here we demonstrate a quasi-equilibrium production method that produces high-quality semiconducting epigraphene (SEG) on macroscopic domains with a band gap of 0.6 eV and room temperature mobilities up to $\mu = 5{,}500\ cm^2 V^{-1} s^{-1}$, which is ten times greater than that of silicon and a factor of 20 greater than that which is theoretically possible with any other 2D semiconductor reported to date[19]. Moreover, SEG is atomically registered with the SiC lattice and

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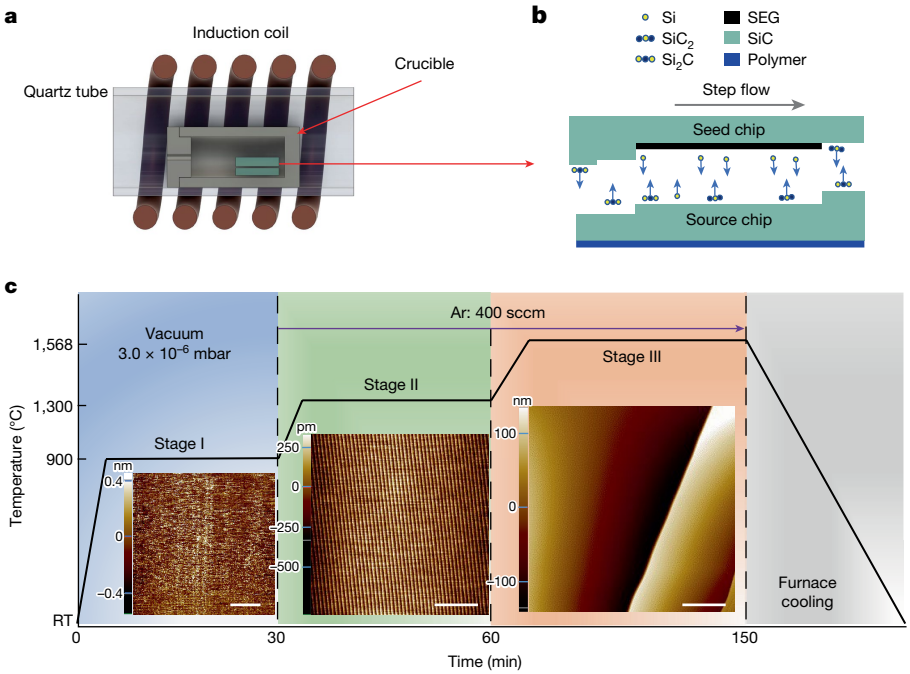

Fig. 1 | SEG production. a, Schematic of a CCS furnace with two 3.5 mm × 4.5 mm SiC chips inside a closed cylindrical graphite crucible that is supplied with a leak inside a quartz tube. The crucible is heated by an eddy current induced by in the coil by a radiofrequency source. **b**, The two chips are stacked with the C face of the bottom chip (source) facing the Si face of the top chip (seed). At high temperatures, a slight temperature difference between the chips causes a net mass flow from the bottom chip to the top chip resulting in the growth of large terraces on the seed chip by step flow and on which a uniform SEG film grows. **c**, SEG is grown in three stages. In stage I, the chip is heated to 900 °C in a vacuum for about 25 min to clean the surface; in stage II, heating the sample to 1,300 °C for about 25 min in 1 bar of Ar produces a regular array of bilayer SiC steps and approximately 0.2-µm wide terraces. SEG-coated (0001) terraces grow in stage III at 1,600 °C in 1 bar of Ar, in which step bunching and step flow produce large atomically flat terraces on which a buffer layer grows in quasi-equilibrium conditions established between the C face and the Si face. The large SEG-coated (0001) terraces are explained in terms of their very large stability. RT, room temperature. Scale bars, 2.5 µm (**c**, stages I and II); 10 µm (**c**, stage III).

patternable using conventional methods, making it an ideal platform for 2D nanoelectronics[8].

SEG production

Conventional epigraphene and buffer layer are grown in a confinement-controlled sublimation (CCS) furnace[16] (Fig. 1a,b), in which a 3.5 mm × 4.5 mm semi-insulating SiC chip is annealed in a cylindrical graphite crucible in an Ar atmosphere of 1 bar at temperatures ranging from 1,300 °C to 1,600 °C (Fig. 1c and Extended Data Fig. 1). The crucible is supplied with a small leak. The rate at which the silicon escapes from the crucible determines the rate at which graphene forms on the surface. Therefore, the growth temperature and the graphene formation rates are controlled. If the leak is sealed, then the graphene growth is strongly suppressed.

Graphene growth can be inhibited in the sandwich method or face-to-face method[5,23] (Supplementary Information), in which two chips are stacked, typically with the Si face of one chip facing the Si face of the other. In 1 bar of Ar, no silicon can diffuse out of the micrometer-scale gap between the chips so that the 1:1 Si:C stoichiometry is maintained, even at high temperatures at which the Si evaporation rates from the surfaces are high. Under these conditions, substantial step flow and step bunching are observed[24] (Fig. 1c and Extended Data Fig. 2). Step bunching is the process in which the substrate surface steps owing to the unavoidable slight miscut of the crystal, which is nominally cut along the (0001) face, merge to produce large atomically flat (0001) terraces bounded by proportionally high steps (Extended Data Fig. 4).

We observe that when the Si face opposes a C face, large atomically flat terraces that are uniformly covered with a buffer layer grow at temperatures around 1,600 °C in an ultrapure Ar atmosphere of 1 bar (Fig. 1c). Although the Si vapour pressure dominates, at $T > 1{,}600$ °C, the vapour pressures of Si_2C and SiC_2 are already sufficient to promote notable SiC transport from the C face to the Si face[25]. This process differs from the conventional nonequilibrium CCS method in which the Si face is continuously depleted of Si. The original experiments (Supplementary Information) were conducted by the Tianjin group using semi-insulating SiC chips in which the bottom chip (Fig. 1) was coated with a polymer to produce large SEG-coated (0001) terraces (Supplementary Information). The graphitized polymer probably causes the bottom chip to become slightly hotter (see below). Samples produced by this method were used in the transport measurements reported here.

The face-to-face method is closely related to the physical vapour sublimation process for silicon carbide crystal production in which the source SiC crystallites at high temperatures in an Ar-filled graphite crucible sublimate and the vapours condense on a cooler SiC seed crystal to produce perfect SiC crystals with large terraces[26], so the large terrace formation can be expected in our system.

The most relevant parameters are the temperature T, the temperature difference between the chips ΔT and the annealing time t, which is typically 1–2 h for $T = 1{,}600$–$1{,}700$ °C. The temperature difference ΔT depends on the crucible design, which is estimated to be of the order of 10 °C, to provide a vapour pressure differential between the two chips required for sufficient mass transport (Methods and Extended Data Fig. 1c). Guided by these principles, alternative crucible designs, chip configurations and annealing processes were tested that do not require a polymer-coated chip (see also Methods and Supplementary Information).

In summary, we found evidence that a thin Si film forms on the hotter C face, in the C face to Si face configuration, whereas large SEG-coated (0001) facets grow on the Si face. Therefore, Si that is missing from the

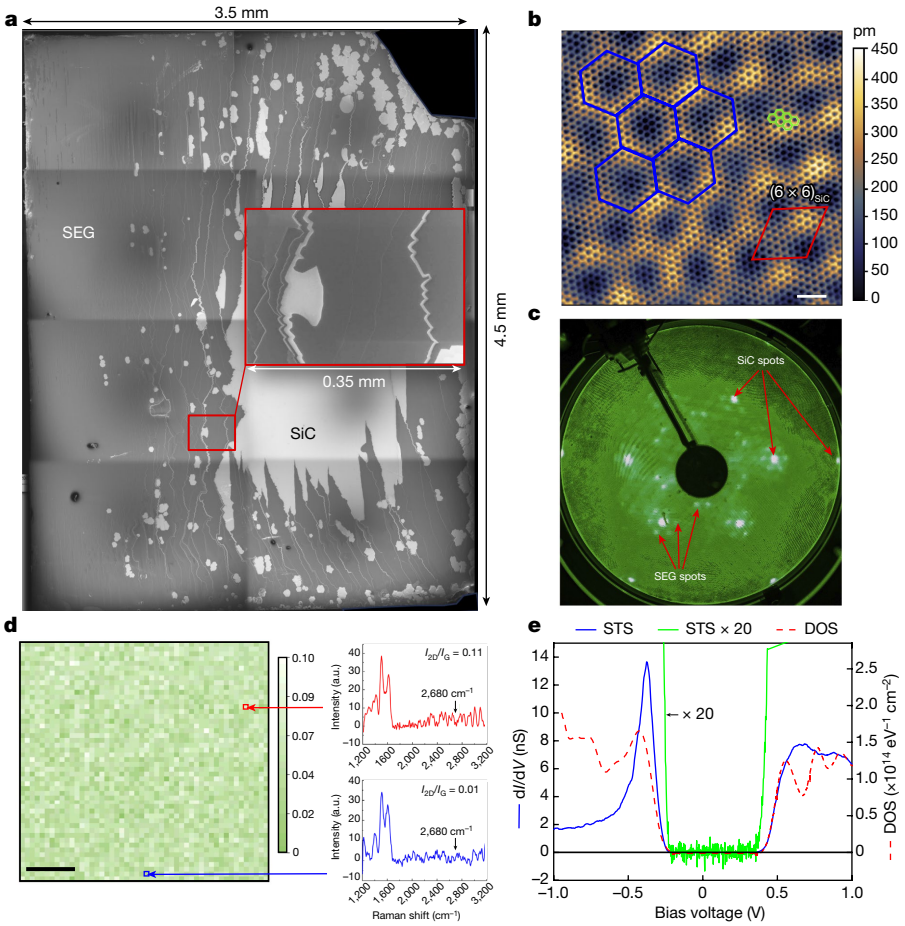

Fig. 2 | SEG characterization demonstrating high coverage of well-ordered, graphene-free, crystallographically aligned SEG, with a well-defined bandgap. a, Composite electron microscope image of a full 3.5 mm × 4.5 mm wafer. The SEM is tuned to provide a vivid contrast between SiC (white areas) and SEG (grey areas). Approximately 80% of the surface is covered with SEG. Graphene would show up as dark patches (the black spots seen here are dust particles). The largest step-free areas are about 0.5 mm × 0.3 mm. **b**, Low-temperature atomic resolution STM image of SEG showing the graphene honeycomb lattice (green) that is spatially modulated with a $(6 \times 6)_{SiC}$ superperiodic structure (red rhombus and purple hexagons) corresponding to the SEG height modulation of about 100 pm (ref. 4) because of the partial covalent bonding to the substrate. **c**, LEED of SEG showing the characteristic $6\sqrt{3} \times 6\sqrt{3}$ R30° diffraction pattern of the SEG lattice, which shows its graphene-crystal structure and the crystallographic alignment of the SEG with respect to the SiC substrate atoms. There is no trace of graphene that is abundant in conventionally produced buffer-layer samples. **d**, Raman map of a 50 µm × 50 µm area with a resolution of 1 µm measuring the intensity ratio I_{2D}/I_G at 2,680 cm^{-1} and at 1,620 cm^{-1}. For graphene, $I_{2D}/I_G \approx 2$. The red arrow corresponds to the red spectrum taken at the spot at which the intensity ratio is the largest in the 2,500 cm^{-1} spectra in the map demonstrating the absence of any graphene on the surface as confirmed with other probes. **e**, Low-temperature STS of SEG, showing the 0.6 eV band gap of SEG (blue line) compared with the calculated DOS of SEG (red dashed line). There is no measurable intensity in the gap indicating a low density of impurity states. a.u., arbitrary units. Scale bars, 1 nm (**b**); 10 µm (**d**).

Si face, may condense on the C face to conserve the stoichiometry. Experimentally, only SEG is formed, and there is no evidence of graphene. We also find that large SEG-coated (0001) terraces also form on the Si face, when the temperature gradient is inverted so that the Si face is hotter than the C face and mass transport is from the Si face (source) to the C face (seed). Apparently, in this inverted crystal growth, the substrate steps evaporate from the source to leave large (0001) terraces on the Si face. Furthermore, in an Si face-to-face configuration, we find that the large SEG-coated terraces form on the hotter Si face and not on the cooler Si face. Moreover, in experiments using a single chip and in which bulk silicon is introduced into the crucible to produce a silicon-vapour-saturated environment in the crucible, the Si face of the chip is partly coated with SEG (Methods and Extended Data Fig. 3) and no graphene is found on the C face.

From these experiments, we conclude that the SEG-coated (0001) facet is more stable than any other SiC facet and, specifically, more stable than a bare (0001) face, implying that in principle it should be possible to produce wafer-scale single-crystal SEG.

SEG characterization

SEG is investigated on all relevant length scales. On the 100 nm to the 1 mm scale, scanning electron microscopy (SEM) provides a high contrast that distinguishes bare SiC, SEG and graphene[27] (Fig. 2a). On the nanometre scale, graphene and SEG are also readily identified in scanning tunnelling microscopy (STM) by its SiC_{6x6} modulation (Fig. 2b). Low-energy electron diffraction (LEED) is used to identify SEG and to verify its atomic registration with the SiC substrate[2] (Fig. 2c). LEED is also used to distinguish SEG from graphene[2]. Raman spectroscopy (1–100 µm) is very sensitive to graphene and SEG, and traces of graphene are easily identified by its intense characteristic 2D peak[28,29] (Fig. 2d). Lateral force microscopy (LFM) distinguishes SEG from SiC and graphene in 10-µm scale scans. Atomic force microscopy (AFM), SEM and optical microscopy can reveal surface steps. AFM is used to measure the amplitude of the steps (Extended Data Fig. 4). Using a combination of these measurements, we find that there is no evidence for graphene either on the plateaus or on the substrate steps in samples

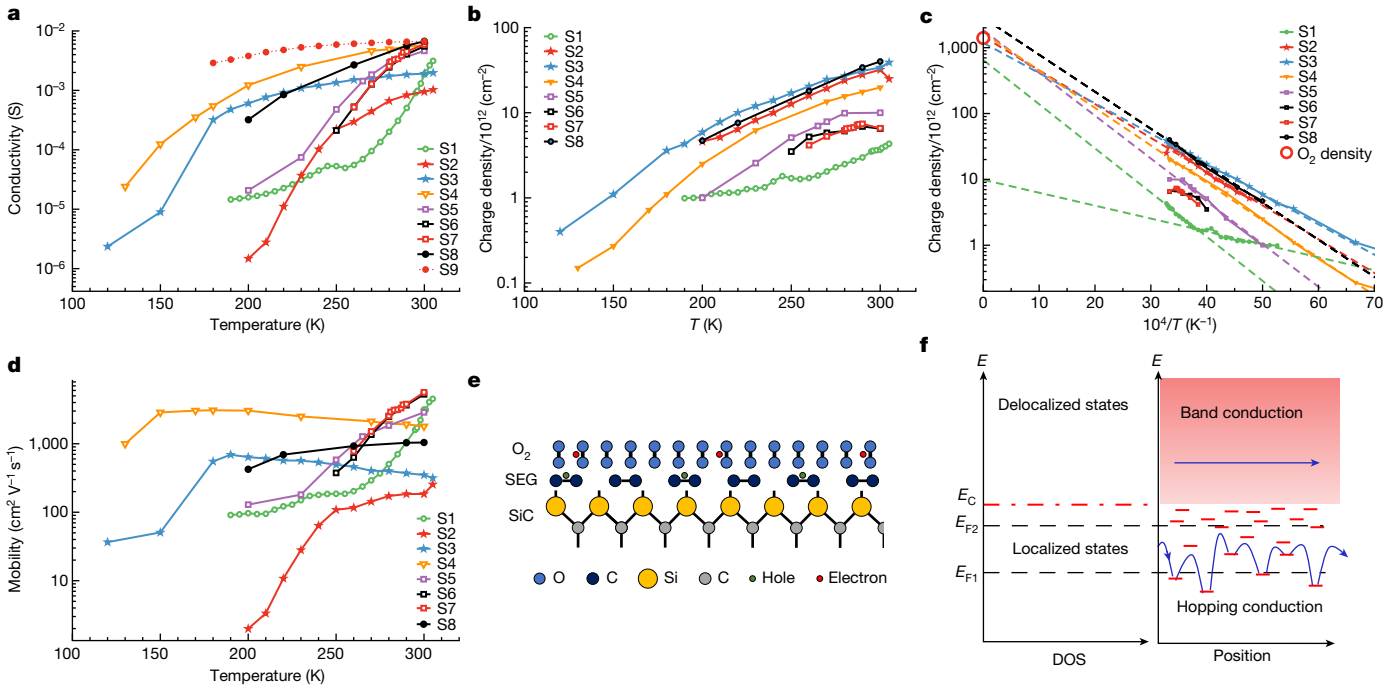

Fig. 3 | Transport properties of oxygen-coated SEG Hall bars. a, The increase in conductivity with increasing temperature is attributed to the increasing ionization of an adsorbed monolayer oxygen on the surface. **b**, Charge density versus temperature. **c**, Arrhenius plots of charge density versus inverse temperature (equation (2)). The uniform slopes are consistent with an activation energy of 120 meV for the thermal ionization of the physisorbed oxygen. Linear extrapolations converge to about $1{,}500 \times 10^{12}$ cm^{-2} corresponding to the density of an oxygen monolayer (large red circle). The reduced low-temperature slope of sample 3 is consistent with a 60% coverage of residual photoresist with a 10-meV activation energy. **d**, Hall mobilities with dramatic increase with increasing temperature (2–5,500 cm^2 V^{-1} s^{-1}) as explained below. **e**, Thermal charge transfer of electrons (red dots) from the SEG to the oxygen monolayer (oxygen) causing the SEG to become hole-doped (green dots). **f**, Transition from low-mobility hopping transport using localized states in the band gap to high-mobility band transport, shown here in terms of electron transport (hole transport is formally equivalent). Similar processes occur in semiconductors in which defects produce localized impurity states in the band gap. At low temperatures and charge densities, the Fermi level is in the bandgap (E_{F1}) and transport is dominated by hopping from one localized state to the other resulting in low mobilities. With increasing temperature, the charge density increases as shown in **b**, causing the Fermi level to rise above the conduction band edge (E_C) so that the transport transitions to high-mobility band transport. Therefore, the transition charge density (and hence the transition temperature) depends on the defect density, which is about 0.27×10^{11} cm^{-2} for sample 4, 4.3×10^{12} cm^{-2} for sample 3 and 17×10^{12} cm^{-2} for sample 2. Details of the various samples are explained in the text.

produced in the face-to-face method as described here. As shown in Fig. 2a, the surfaces are either coated with SEG or they are bare SiC. Figure 2e shows a cryogenic STM image that maps the density of states (DOS) of SEG as a function of the Fermi energy. The image shows a well-defined band gap of 0.6 eV. There are no detectible states in the band gap in contrast to the buffer-layer samples produced by the conventional sublimation methods[22].

SEG transport properties

Preliminary measurements of top-gated field-effect transistors (Methods and Supplementary Information) showed ambipolar properties with an on–off ratio of about 10^4. However, the mobility is only 22 cm^2 V^{-1} s^{-1}. It is limited by scattering from the top-gate dielectric that led to the investigation of SEG devices doped by charge transfer from adsorbed molecules to exhibit the intrinsic transport properties of SEG.

A series of transport measurements on SEG Hall bars were patterned using two different methods. The samples were p-doped with ambient air in pure oxygen or in pure oxygen and with ultraviolet radiation. In this way, room temperature charge densities n from $n = 4 \times 10^{12}$ cm^{-2} to 4×10^{13} cm^{-2} were achieved. We are specifically interested in oxygen doping because it markedly p-dopes the buffer layer (and SEG), and it is the only atmospheric gas that is stably absorbed on the buffer layer as demonstrated in a previous study[5]; annealing at 400 °C in a vacuum is required to desorb the oxygen (see also Supplementary Information).

The measurements were performed in a cryostat superconducting magnet at temperatures ranging from 100 K to 300 K. At each temperature, the magnet was swept from $B = -3$ T to +3 T for Hall measurements to determine the charge densities. Conductivities σ were determined from four-point measurements, and the Hall mobilities μ were determined from $\sigma = ne\mu$, where e is the electric charge. In 2D materials, resistivities are expressed in ohms and conductivities in siemens.

The conductivities of the samples (Fig. 3a) show a monotonic increase with increasing temperature. The room temperature conductivities range from 1×10^{-3} S to 8×10^{-3} S corresponding to resistivities ρ from 125 Ω to 330 Ω. The low-temperature values are up to a factor of 1,000 smaller. Charge densities (Fig. 3b) range from about 0.2×10^{12} cm^{-2} to 40×10^{12} cm^{-2}. The STS measurements (Fig. 2e) show that SEG is intrinsically charge neutral, so that the charging is caused by environmental gasses (including trace volatile organic compounds) and by residual resistance from lithographic processing[30]. The mobility (Fig. 3c) generally increases with increasing temperature tending to saturate at higher temperatures. The maximum measured mobility is 5,500 cm^2 V^{-1} s^{-1}. The room temperature SEG conductivities, charge densities and mobilities are all within the ranges that are typical for epigraphene. However, the temperature dependences are similar to that of a doped semiconductor with deep acceptor states as elaborated below.

A semi-log plot of the charge densities plotted as a function of $10^4/T$ in Fig. 3c shows Arrhenius behaviour. Note that the charge density n of a p-type semiconductor with a doping density of N_0 is given by[31]

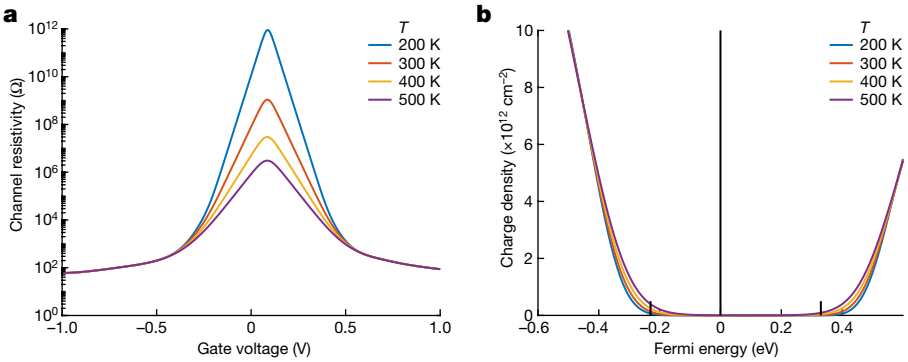

Fig. 4 | Predicted SEG field-effect characteristics. a, Predicted SEG channel resistivity using the calculated DOS, with an SEG mobility of 4,000 $cm^2 V^{-1} s^{-1}$ assuming an ideal dielectric, which predicts a room temperature on–off ratio that exceeds 10^6. **b**, Charge density versus E_F. The turn-on voltages for the N and P branches at $T = 300$ K are predicted to be +0.34 V and −0.23 V, respectively.

$$n = \frac{N_0}{1 + g \times \exp\left(\frac{E_A - E_F}{kT}\right)} \quad (1)$$

where k is the Boltzmann's constant, E_F is the Fermi level, E_A is the acceptor energy level and g is the acceptor degeneracy. For a level with $g = 1$, at low temperatures ($E_A - E_F \gg kT$),

$$n \approx N_0 \exp\left(-\frac{\Delta E}{kT}\right) \quad (2)$$

Equation (1) is derived for the ionization of acceptor states in a semiconductor[31], but the thermodynamics is similar for the ionization of neutral molecules on a 2D surface. From Fig. 3c, we find that $\Delta E = 0.12 \pm 0.02$ eV. We also find that $N_0 \approx 1.500 \times 10^{15}$ cm^{-2}, which is close to the estimated oxygen density of an oxygen monolayer[32] (that is, 1.400×10^{15} cm^{-2}; Fig. 3, large red circle) consistent with the model that the p-doping is because of an approximately complete oxygen monolayer. Variations in ΔE and N_0 are probably caused by partial coverage of trace environmental volatile aromatic molecules that are readily absorbed on graphitic materials reducing the oxygen coverage and affecting its ionization energy[33]. The two slopes observed in sample 1 (Fig. 3d) are probably because of a significant (about 60%) coverage of residual photoresist material that causes the p-doping of SEG[34] at the low temperatures because of its small $\Delta E = 0.035$ eV as determined from the slope.

The mobilities of samples 2, 3 and 4 show a steep rise followed by a plateau at transition temperatures $T_{tr} = 250$ K, 190 K and 150 K, respectively. The corresponding transition charge densities n_{tr} are 17×10^{12} cm^{-2}, 4.3×10^{12} cm^{-2} and 0.27×10^{12} cm^{-2}. The mobilities at low charge densities are because of localized defect states in the band gap[35] (Fig. 3e,f). The localized states are filled as the charge density is increased, after which the transport transitions to high-mobility band transport so that n_{tr} is a measure of the density of the defect state. This process has been observed in 2D semiconductors[35], and it contributes to the subthreshold rise in thin film transistors[36]. In CCS-produced buffer layers, the transport in the bandgap has been identified as variable-range hopping[5] (Supplementary Information).

Sample 4 was produced with a shadow mask that explains its small defect density. Sample 9 (Fig. 3a) was produced by draping four gold-leaf contacts over an unprocessed ribbon and its conductivity is large and similar to that of sample 4; however, it was not in a Hall bar configuration so that its charge density and mobility could not be measured. Sample 2 was produced using oxygen and ultraviolet light exposure, which explains its large defect density and relatively low mobility. The decreasing mobility with increasing charge density in the post-threshold plateau of samples 2–4 is reminiscent of charge impurity scattering in graphene[37]. Samples 5–7 have large mobilities that increase with increasing temperature and a charge density that seems to saturate, which we do not understand at present.

From the measured semiconducting and the DOS, we can predict the response of a field-effect transistor (Fig. 4). The channel conductivity can be expressed as $\sigma(V_g) = n_e e\mu_e + n_h e\mu_h$, where n_e is the electron density and n_h is the hole density[38]:

$$n_{e,h}(E_F, T) = \pm \int_{E_F}^{\pm\infty} D(\varepsilon) F_{e,h}(E_F, T, \varepsilon) d\varepsilon \quad (3)$$

where $F_{e,h}$ are the electron and hole Fermi functions and DOS $D(\varepsilon)$ is from Fig. 3c (red dashed line), with $\mu = 4{,}000$ $cm^2 V^{-1} s^{-1}$, an on–off ratio of 10^6 (Fig. 4a) and a subthreshold slope of 60 mV per decade (Fig. 4b), which are sufficient for digital electronics[39]. An actual SEG field-effect transistor is shown in the Methods in which the on–off ratio is already 10^4, but its field-effect mobility μ_{FET} is only 22 $cm^2 V^{-1} s^{-1}$ primarily because of the disorder caused by the dielectric and large Schottky barriers at the contacts.

Conclusion

The exclusive focus of epigraphene nanoelectronics research, predating mainstream graphene research[40,41], was to develop a 2D nanoelectronics platform to succeed in silicon electronics[8]. The lack of a band gap in graphene was considered to be the main hurdle[39]. Here we have demonstrated that a well-crystallized buffer layer is an excellent 2D semiconductor with a band gap of 0.6 eV and with room temperature mobilities larger than that of all current 2D semiconductors. A prototype FET has an on–off ratio of 10^4 (Methods and Extended Data Fig. 8), which may reach 10^6 in optimized devices.

SiC is an important commercial semiconductor that is compatible with conventional microelectronics processing methods[42] and THz applications[43]. Moreover, epigraphene can be nanopatterned, which is not possible with graphene on other substrates because of pervasive edge disorder[44]. By contrast, the epigraphene edges turn out to be excellent one-dimensional conductors[45]. SEG can be intercalated with a wide range of atoms and molecules to form a wide range of materials with useful electronic and magnetic properties[46].

Future work will primarily focus on reliably producing macroscopic terraces with viable dielectrics that do not severely reduce the mobility[47,48], managing the Schottky barriers and developing schemes to produce integrated circuits. In the Methods, we briefly touch several of these points, where we convert SEG into quasi-free-standing graphene (Extended Data Figs. 5 and 6) by intercalating hydrogen[49] so that seamless SEG and quasi-free-standing graphene junctions are

realized mitigating interconnect problems[17] (Methods, Extended Data Fig. 7 and Supplementary Information). In conclusion, SEG provides opportunities in 2D nanoelectronics with a marked potential to become commercially viable in the future.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41586-023-06811-0.

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Methods

SEG production

SEG-coated SiC chips used for transport measurements were produced in a closed cylindrical high-purity graphite crucible, 14 mm long and 10 mm in diameter with a bore size of 5.5 mm. The crucible is closed with a cap with a 1-mm hole (Fig. 1a). The crucible is placed in a quartz tube and heated inductively. The temperatures are monitored and controlled using an optical pyrometer. The typical sandwich is composed of two 3.5 × 4.5 mm SiC chips, in which the Si face of the top chip (seed) faces the C face of the bottom chip (source). The Si face of the source chip (specifically not between the chips) may be coated with a polymer that most probably causes its temperature to be slightly higher than that of the top chip.

The sandwich is placed in the crucible and annealed in three phases as shown in Fig. 1. In the first phase, they are cleaned of surface contaminants in high vacuum at 900 °C followed by a high-temperature pre-growth annealing step at 1,300 °C, in 1 bar of ultrahigh-purity Ar. This causes the surface of the Si face of the top chip to develop a regular stepped structure (Fig. 1c, middle). In the final annealing step at about 1,600 °C, the Si face of the top chip develops large atomically flat terraces (Fig. 1c, right) that are covered with a buffer layer (Fig. 2a).

The graphitized polymer helps in establishing the required temperature differential between the top and the bottom chips. However, similar results have also been obtained without the polymer coating in a vertical furnace (Extended Data Fig. 1a) in which the temperature gradient is controlled by the location of the sandwich in the crucible. A specific temperature difference within the relatively narrow annealing temperature window is found to be important. Although nominally the C face of the bottom chip is free of graphene, it becomes fully covered with graphene, with certain polymer coatings (Supplementary Information). The Si face of the top chip always has a buffer layer covered with step-free terraces; the covering is not always complete, especially in the middle of the chip. This may be because of an increased Si vapour pressure. The size of the terraces and buffer-layer coverage varies considerably depending on the temperature and annealing time, polymer coating, SiC doping, SiC polytypes and miscut size and direction. Current research focuses on optimizing these parameters, as well as developing alternative crucible designs in which the temperature gradient is better controlled and with chips supplied with corrals that define growth areas[50].

Extended Data Fig. 1a shows an alternative crucible design to study the effects of the temperature gradient in which the gradient increases from the middle to the top of the crucible, as confirmed by numerical simulations of the temperatures. This configuration is also used to demonstrate the mass transport from the hotter source chip to the cooler seed chip. For example, Extended Data Fig. 1b shows optical images of the surfaces of the Si-face seed chip superimposed on a mirror image of the C-face source chip, which shows their complementary nature: material that is removed from the hotter C-face chip is deposited on the cooler Si-face chip. The C-face image has been shifted slightly for clarity. We also find that when the temperature gradient is inverted, the Si face is still covered with SEG (however, the terraces are small). This further verifies that the SEG-covered Si face is remarkably stable.

Extended Data Fig. 2 shows inverted growth of SEG. Here we see that the source chip (Extended Data Fig. 2a) has relatively small regular terraces (about 10 μm) that are covered with SEG (darker areas), whereas in the seed chip, (Extended Data Fig. 2b) the surface is irregular. Contrast-enhanced optical images of the source chip (Extended Data Fig. 2c) show a regular array of parallel substrate steps, whereas the step structure is highly distorted on the seed chip. Note that the large steps (dark lines) of the source chip are mirrored on the seed chip, which suggests that the source chip surface morphology is imprinted on the seed chip. Hence, in contrast to the Si-face to C-face configuration, large terraces do not form on either chip. Moreover, SEG forms on the source chip rather than on the seed chip.

We further find that SEG is stable in saturated silicon vapour. To show this, we placed a single chip in a closed graphite crucible that had been saturated with silicon. As shown in Extended Data Fig. 3a, after annealing the Si face is covered with SEG (darker areas); however, the terraces are small.

We have also observed that in the standard C-face source to Si-face seed configuration, Si is deposited on the C-face, whereas SEG forms on the Si face.

These observations lead us to conclude that the SEG-coated (0001) face is much more stable than the bare (0001) face and much more stable than all other SiC crystal faces. That is why when SiC is deposited from the C-face source – in which the evaporation rates are known to be larger than from the Si-face – the newly deposited material favours SEG-coated (0001) facets.

Surface characterization

SEG and QFSG samples were characterized using an AFM (Park Systems NX10 with 50 × 50 μm scanning range) in non-contact mode for topology and contact mode for LFM measurements to identify graphene (Extended Data Fig. 4). Microscopy measurements were done using an SEM (Hitachi SU3500, 15 kV). Raman spectrometry was performed using a 532-nm laser with a spatial resolution of 1 μm (Fig. 2d). STM and STS measurements were taken using a cryogenic scanning probe microscope (PanScan Freedom) (Fig. 2b,e). LEED measurements were taken at the Georgia Tech Epigraphene Keck Lab (Fig. 2c). The representative SEM chip image (Fig. 2a) was made with a LEO 1530 FE-SEM (2 nm resolution), at 3 kV in in-lens mode.

Extended Data Fig. 4 (top and middle) shows an SEM image of an atomically flat (0001) 300-μm wide terrace between two 100-nm high steps. An LFM scan was taken over the width of the terrace (white dotted line). No substrate steps were observed in that scan. Furthermore, 10 μm × 10 μm LFM maps were made at three locations (a, b and c), and no substrate steps or graphene patches were found, which confirms the SEM image and Raman spectroscopy of the terrace.

Sample production

To produce Hall bars, photoresist S1805 was spin-coated on the Si face of the top chip, which was then photolithographically patterned using a direct laser writer (SVG-Micro 100).

Bare SEG samples were heated to 200 °C for 20 min and rapidly cooled to room temperature in a nitrogen flow. Subsequently, 3.5 μL of S1813 photoresist was spin-coated on the 3.5 mm × 4.5 mm SiC chips and subsequently heated to 115 °C for 1 min. The samples were then exposed to a 405-nm laser using a 50× objective lens in 25 ms steps, after which the sample was heated to 120 °C for 2 min. The exposed samples were developed in a 6 wt% sodium hydroxide solution for 19 s at 22 °C after which they were baked at 110 °C for 10 min.

After e-beam metal deposition, the sample was soaked in acetone for at least 24 h. During that time, the acetone was refreshed several times. An acetone-filled syringe was used to accelerate the lift-off process. After the lift-off was complete, the samples were rinsed in isopropanol and dried in a purified dry nitrogen flow.

Samples 6 and 7 were subsequently oxygen-doped by exposure to air. Sample 5 was treated with oxygen and ultraviolet light. The oxygen flow was 0.1SCCM, and the sample was kept under ultraviolet radiation for 2 min at room temperature. We chose oxygen because it is safe, easy to use and stable on SEG as has been previously demonstrated[5] (Supplementary Information). Moreover, the charge densities can be varied over an order of magnitude, and it is easily removed by annealing in a vacuum at moderate temperatures. By contrast, ammonia, (n-dopant) similar to several other graphene dopants, rapidly desorbs at room temperature[5] (Supplementary Information). Other dopants will be studied in future comprehensive investigations under controlled conditions.

Contacts and gate electrodes were produced from 10 nm Cr and 30 nm Au e-beam (EB-500)-deposited films followed by lift-off. Alumina

dielectrics were produced by e-beam deposition of 2 nm Al that was oxidized in residual oxygen, which served as the seed layer for the subsequent ALD process. Hall bar structures were typically 300 μm long and 30 μm wide.

Alternatively, the electrodes on samples 4 and 8 were patterned using 20–30 μm stainless steel or copper shadow masks that were patterned with a focused femtosecond laser. The samples produced using shadow masks have markedly smaller defect densities demonstrating the important role of contamination in the lithography processes (that is, sample 4; Fig. 3).

Sample 1 was produced by selecting a naturally occurring long SEG ribbon that was contacted with prefabricated gold-leaf strips using a micromanipulator.

Transport measurements

Measurements were made on the top-gated samples and on oxygen-doped samples. The latter is important to get a high lower bound of the intrinsic mobility and other transport properties of SEG, which top-gated samples cannot provide because of the severe scattering caused by the dielectric.

Cryogenic transport measurements reported in the main text were taken using an Oxford Instruments cryostat, Teslatron PT (300 mK to 305 K) with a maximum magnetic field of 14 T. Measurements were taken using a Keithley 2450 SourceMeter, a Stanford Research SR560 voltage amplifier, a SR830 lock-in amplifier, a voltage amplifier and a DL Instruments 1211 current preamplifier. Four- and two-point measurements were conducted at temperatures ranging from 120 K to 305 K. For each measurement, the temperature was well stabilized, and the magnet was swept from −3 T to +3 T.

Measurements were also taken in a cryogenic probe station (Lakeshore-Model TTPX) with a semiconductor device analyser (Keysight-B1500A) for the FET measurements and for the two- and four-point measurements on unprocessed natural SEG ribbons that were contacted using mechanically transferred prefabricated gold-leaf strips (Fig. 3a, sample 9). Although the charge densities of these devices could not be determined, their properties were consistent with highly pure SEG ribbon when compared with the processed samples in Fig. 3.

Quasi-free-standing graphene

SEG was converted to quasi-freestanding graphene (QFSG) by hydrogen intercalation[49,51], which passivates the Si bonds. Surface studies of QFSG (Extended Data Fig. 5) show an essentially perfect graphene lattice structure as expected, and Raman maps confirm that the surface is free of SEG. Transport measurements on QFSG Hall bars (Extended Data Fig. 6) show that at room temperatures, mobilities, charge densities and resistivities are remarkably similar to SEG. However, they are quite different at lower temperatures because of the band gap in the SEG samples. The high mobilities at room temperature are primarily because of the weak electron–phonon interaction[19] and the low defect densities.

QFSG is also important for nanoelectronics because it facilitates a seamless contact between QFSG and SEG, which will be crucial for nanoelectronics because metallic nanoscale contact with SEG will be challenging. Extended Data Fig. 7 shows an example of such a junction, and in Supplementary Information we show transport measurements between graphene and CCS-produced buffer layer. Moreover, a wide range of materials can be intercalated under SEG that can be used to mitigate Schottky barriers between QFSG and SEG as well as provide interconnects in integrated nanostructures.

SEG–graphene junctions

Because metal to graphene contacts are fragile, the concept of semimetallic graphene to SEG contacts has been an essential aspect of epigraphene electronics from the outset[7,17,40]. Examples of SEG–graphene junction are shown in Extended Data Fig. 7 and in Supplementary Information.

SEG field-effect transistor

The electrical properties of the SEG were measured by characterizing a fabricated top-gated SEG FET. Extended Data Fig. 8a shows a schematic of the device. The transfer curves are plotted in Extended Data Fig. 8b with V_{ds} of 0 V, 1.0 V and 2.0 V. The device shows ambipolar characteristics. As V_{ds} increases, both I_{on} and I_{off} monotonically rise. As shown in Extended Data Fig. 8c, the device exhibits reasonable switching performance with an on–off ratio of about 10^4 at $V_{ds} = 1$ V and $I_{on} = 15$ nA. The threshold voltage (V_{Th}) is −0.21 V, which is extracted by extrapolating the linear regime of the transfer curve to the gate voltage axis. The subthreshold swing (SS) is calculated from $SS = dV_{gs}/d(\log(I_{ds}))$ and is about 155 mV dec^{-1}. Extended Data Fig. 8d shows the output curves of the device. There is a substantial barrier, which is clear from the non-linear behaviour of I_{ds} at high V_{ds} and the large contact resistances. Extended Data Fig. 8e extrapolates the linear rise of the output curve to the baseline, which closely corresponds to the band gap (Fig. 2e). Improving the metal contacts and the quality of the dielectric layer will notably enhance the device performance to approach the theoretical values calculated in Fig. 4.

Data availability

The authors declare that all other data supporting the findings of this study are available in the Article and its Supplementary Information and are also available from the corresponding author on request.

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Author contributions J.Z. contributed to SEG growth, transport measurements, data processing and Supplementary Information section 4. P.J. contributed to STM measurements, data processing and Supplementary Information section 4. Y.L. was involved in materials growth and characterizations, transport measurement and data processing. R.L. contributed to device fabrication, transport measurement and data processing. K.Z. was involved in material characterization, device fabrication and data processing. H.T. contributed to material characterization and device fabrication. B.B. assisted in material growth and characterization and transport measurement. L.H. was involved in material characterization and device fabrication. K.Y. contributed to material characterization and device fabrication. X.X. contributed to material growth and characterization. R.M. edited the Supplementary Information section 4. L.M. initialized, conceptualized and supervised the project at TICNN and contributed to material growth, transport measurements, data analysis, Supplementary Information section 4 and editing of the paper. W.G. and N.D. helped with data and production of Fig. 1a, Fig. 2a,c, Fig. 3e, Extended Data Fig. 1a,b, Extended Data Figs. 2,5, Extended Data Figs. 3,6 and Supplementary Information section 1. W.A.d.H. directed the Georgia Institute of Technology projects and the TICNN transport measurements, analysis of Figs. 3 and 4 and Extended Data Fig. 8e and identified and analysed the stable SEG phase and wrote the paper.

Competing interests The authors declare no competing interests.

Additional information
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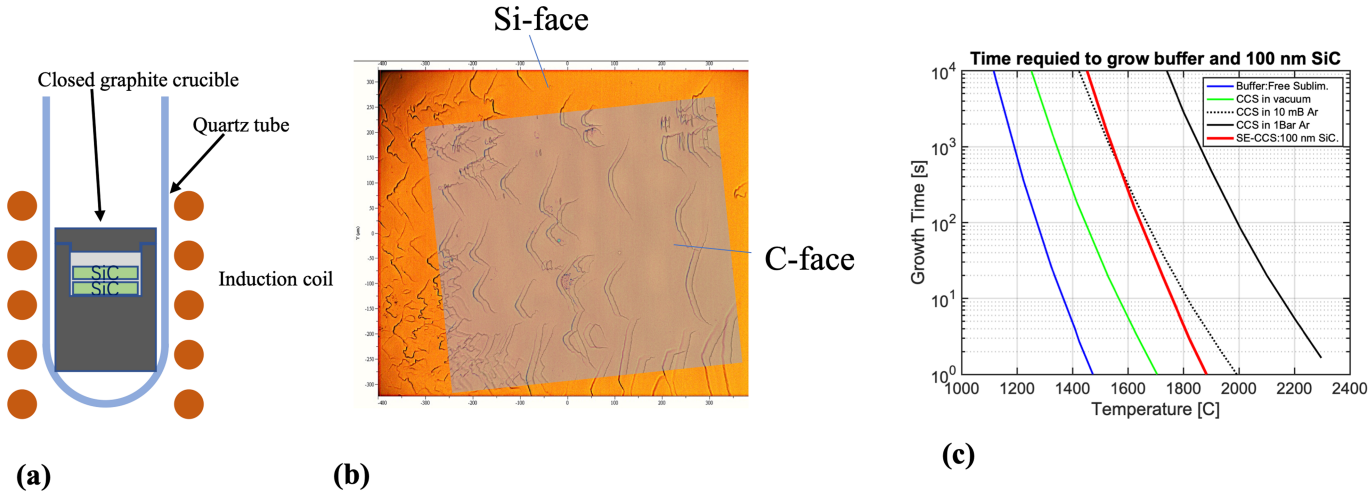
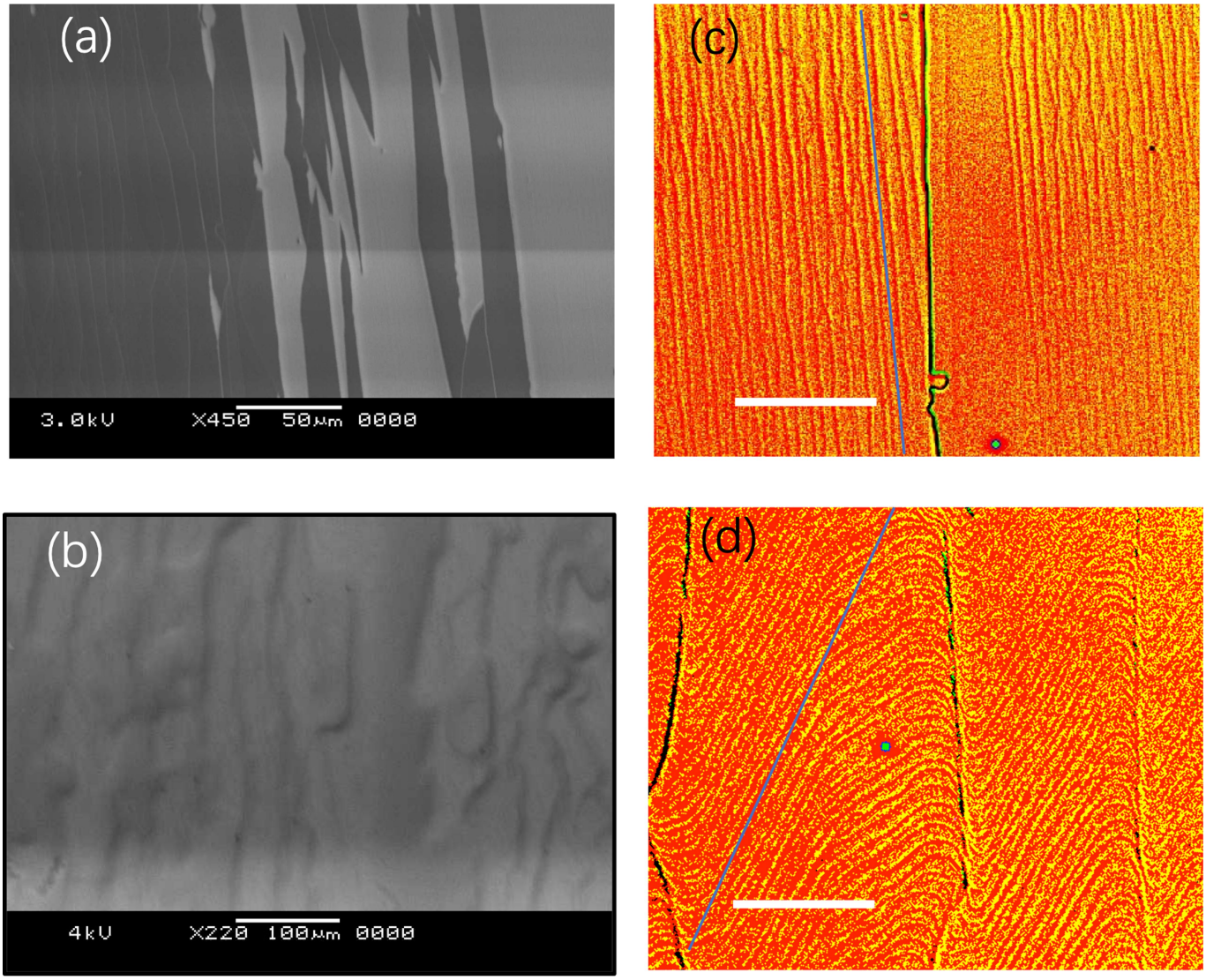
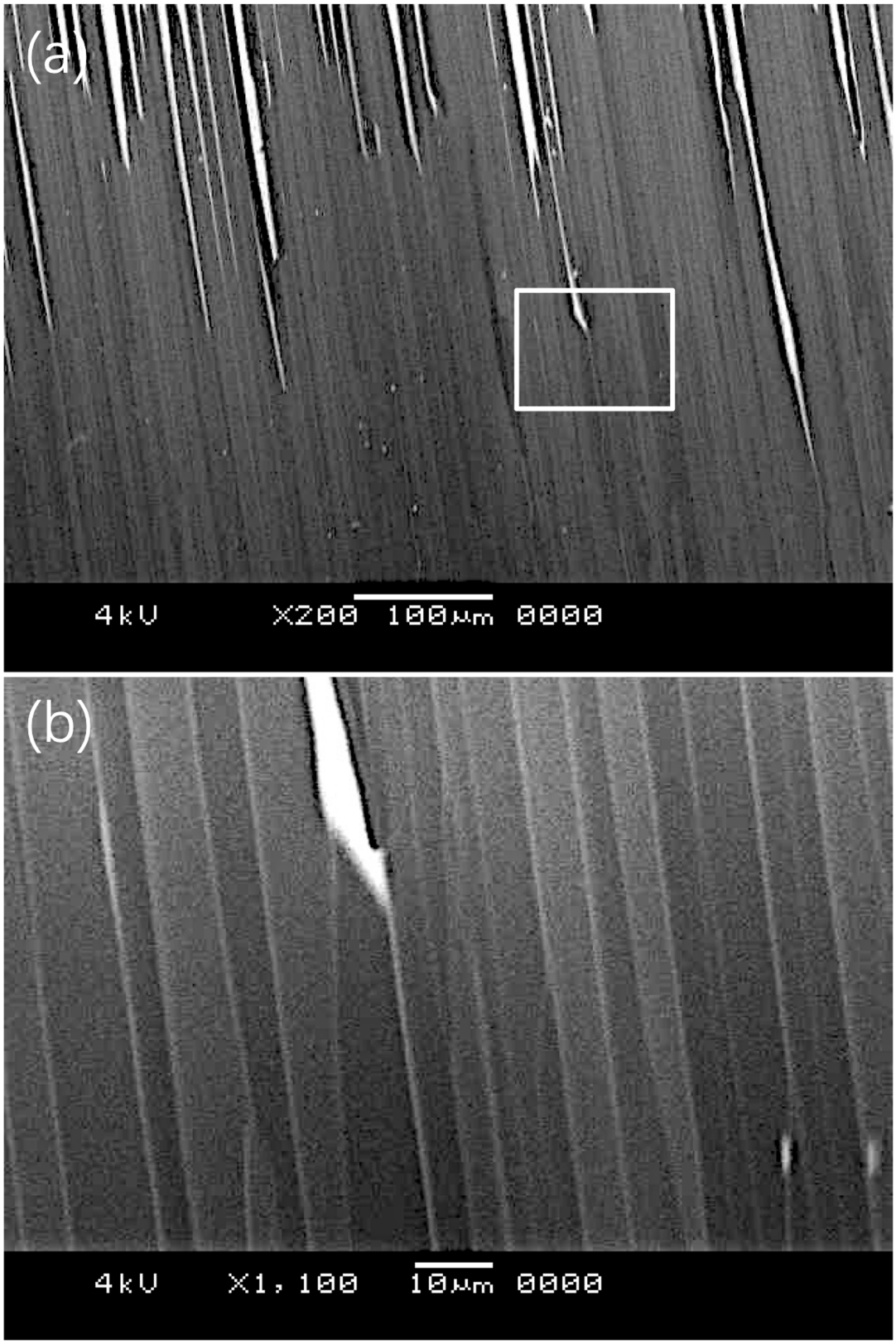


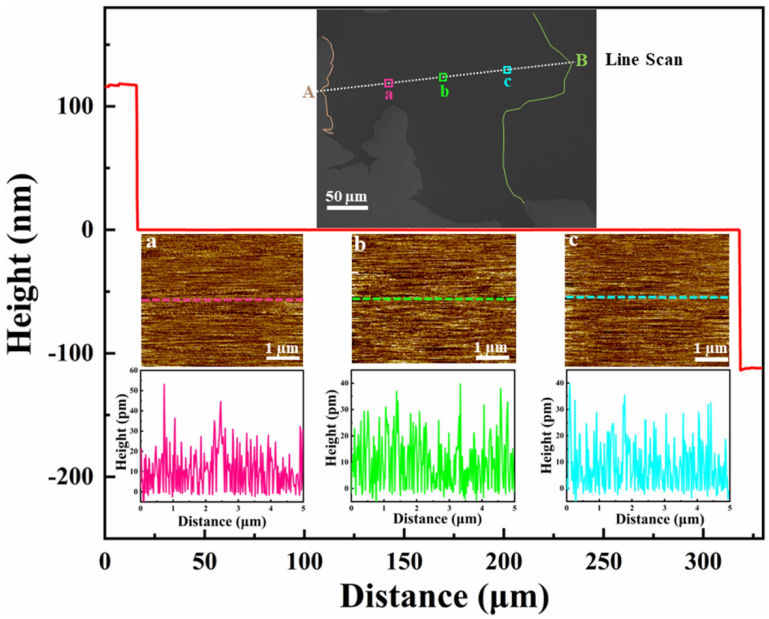
Extended Data Fig. 1 | Face-to-face growth of SEG. (a) Vertical furnace with improved temperature gradient control. **(b)** Overlapped images of the surface of a Si-face seed chip and mirror image of the corresponding C-face source chip (slightly shifted) showing identical complementary topological features, i.e., material removed from the C-face is deposited directly above it on the Si-face which demonstrates the close interaction between the two chips. **(c)** Approximate times to grow a buffer layer and to grow 100 nm SiC from the source chip on the seed chip where the latter is more than 10 C cooler than the former.



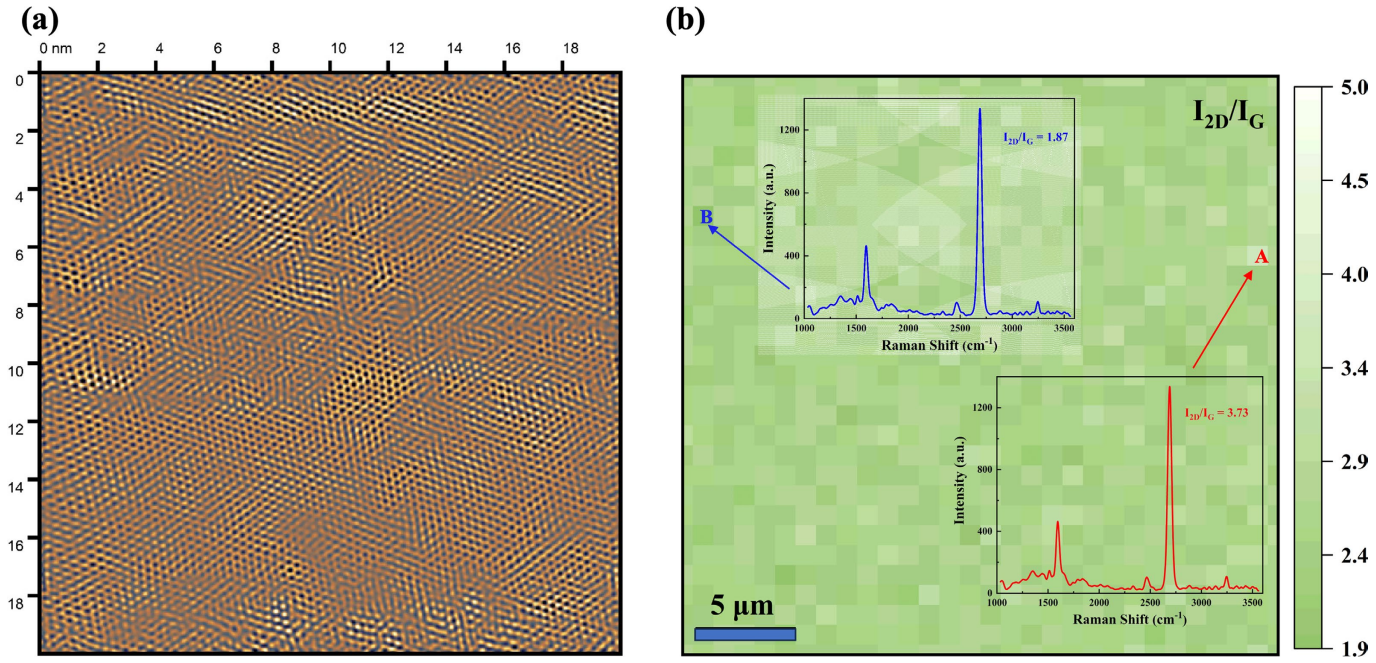
Extended Data Fig. 2 | Si-face source to C-face seed growth. (a) In this inverted geometry SEM images show SEG growth on the Si-face. (b) SEM of the C-face shows an irregular structure. (c) Contrast enhanced optical microscopy shows that the (0001) terraces on the Si-face are small but regular. (d) Contrast enhanced optical microscopy shows irregular step structure on the C-face which appears to be imposed by large steps (dark lines) the Si-face. Blue lines in (c) and (d) indicate the step directions of the unprocessed chips.



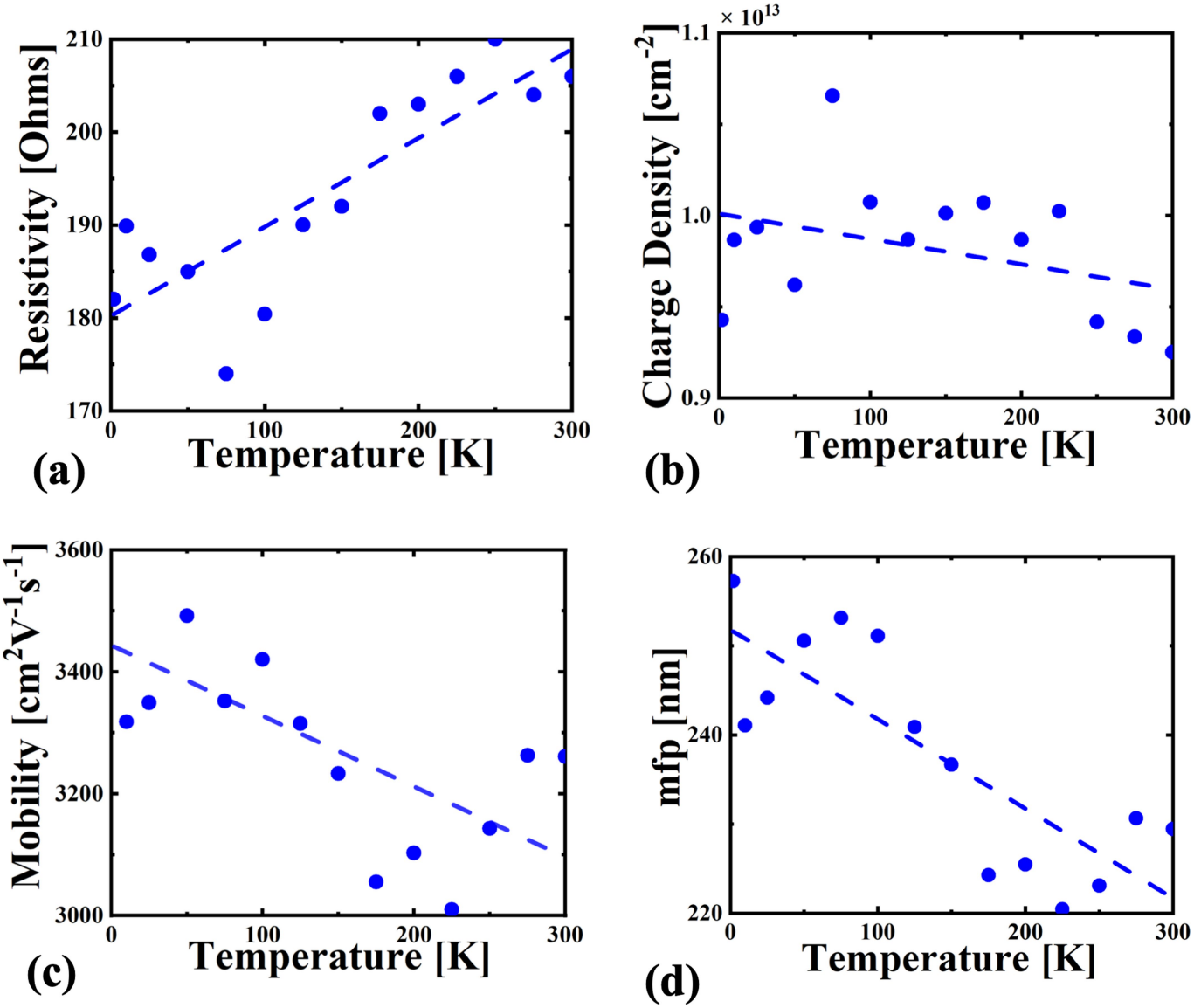
Extended Data Fig. 3 | SEM image a single Si-face of a chip that is processed in a silicon saturated crucible showing the stability of SEG in a Si saturated environment. (a) the surface is largely covered with narrow (0001) terraces covered with SEG (darker areas). The white areas are bare SiC. (b) zoom in of boxed area.



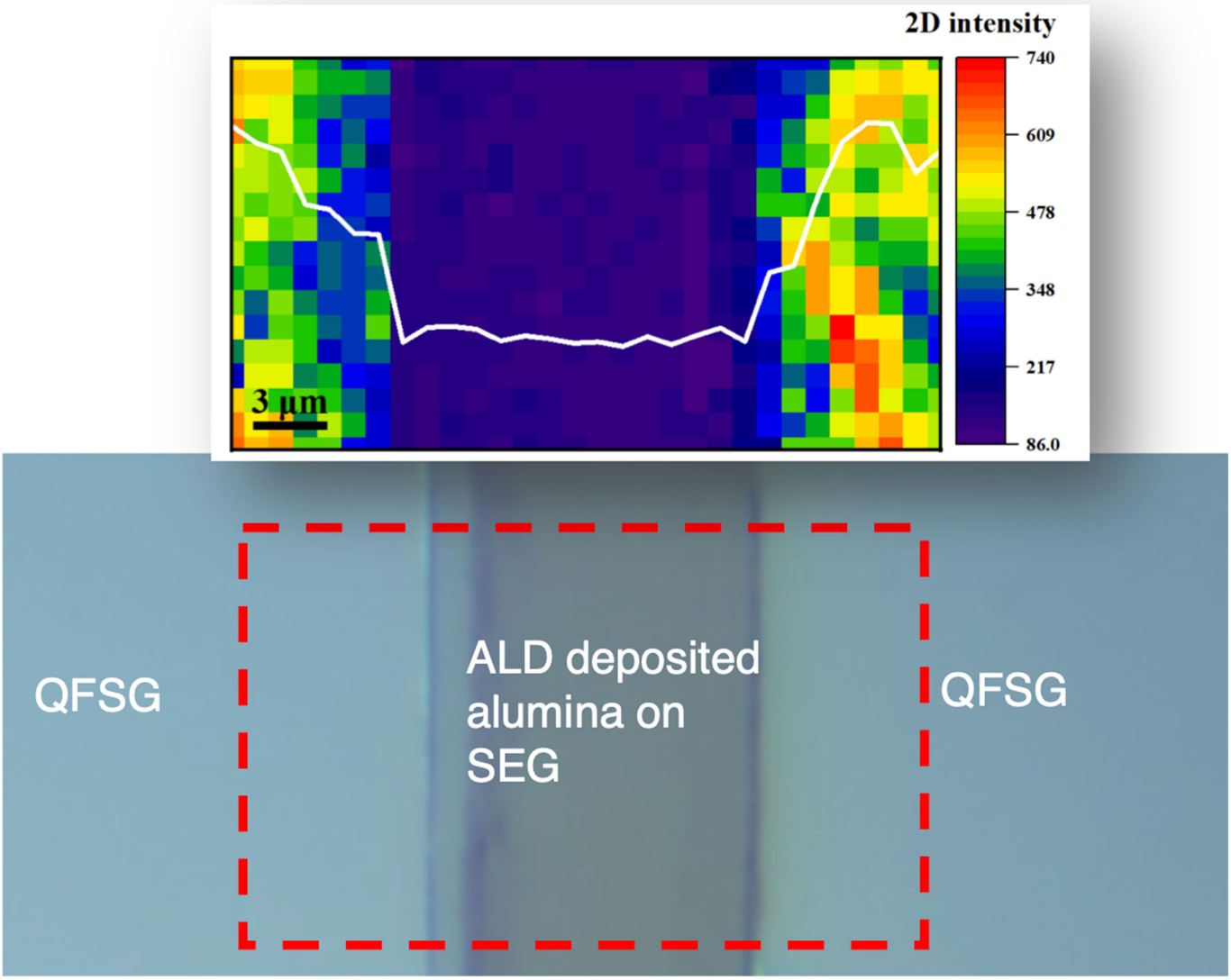
Extended Data Fig. 4 | AFM measurement of an atomically flat SEG terrace between two approximately 100 nm high substrate steps 300 µm apart. In a single line scan, spanning this distance, no SiC steps are detected, (these would be at least 250 pm high.) If there were substrate steps anywhere between the major steps, then this scan would have detected them. Topological 10 µm x 10 µm maps were made at three locations indicated, which did not detect any features larger than 50 pm, i.e., 5 times smaller than the minimal SiC substrate step heights, which verifies that SEG is atomically flat.



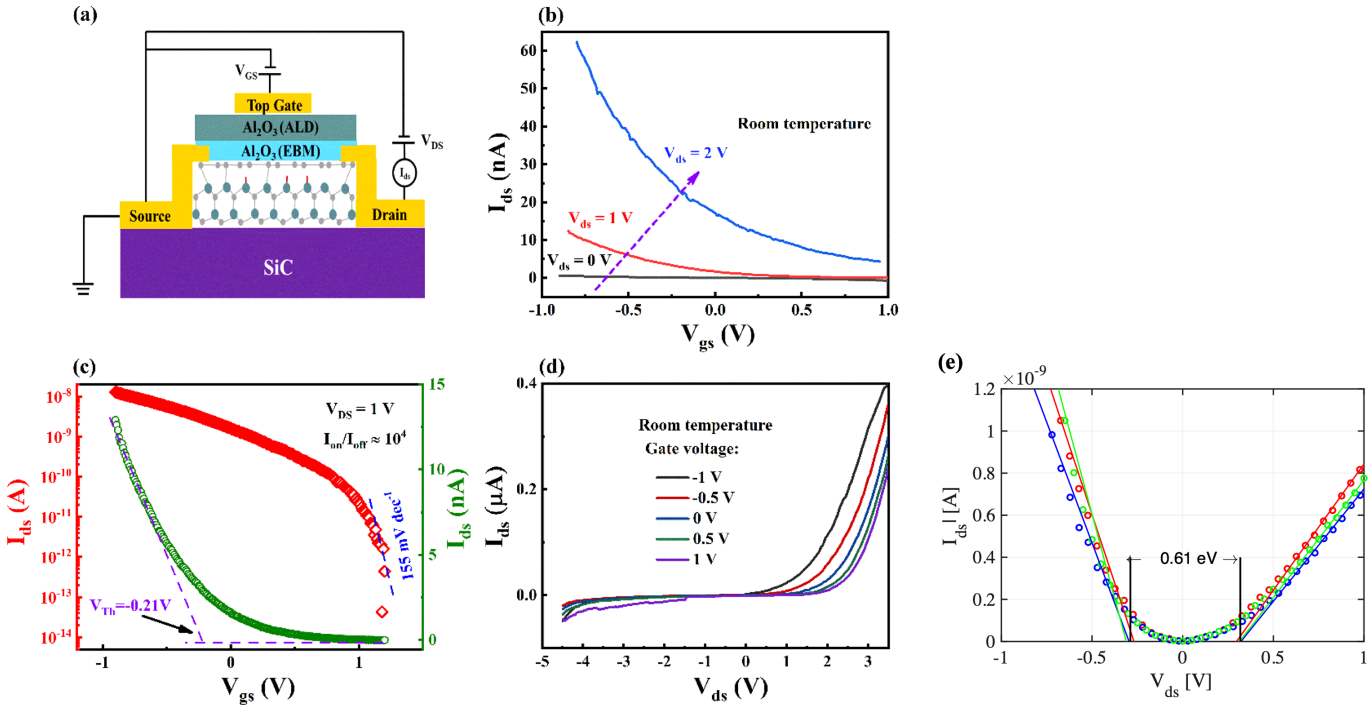
Extended Data Fig. 5 | QFSG characterization. (a) Low temperature STM of a 20 µm by 20 µm area of QFSG produced by hydrogen intercalation shows that it is defect free. (b) Raman map of a 25 µm × 25 µm area shows that it is completely covered with graphene with no bare SiC or buffer. The arrow labeled A points to a region with a $I_{2D}/I_G = 3.73$ (red scan) and the arrow labeled B points to a region with a $I_{2D}/I_G = 1.75$ (red scan). Variations of this magnitude are expected for graphene.



Extended Data Fig. 6 | Transport measurements of a QFSG Hall bar. (a) Resistivity versus temperature, (b) Charge density versus temperature (c) Mobility versus temperature. (d) Mean free path versus temperature. Note the absence of a significant temperature dependence compared with SEG (Fig. 3). Also note that at room temperature, the charge densities and the mobilities are comparable to those of SEG.



Extended Data Fig. 7 | Example of a seamless SEG/QFSG junction. The junction was produced by depositing an Al_2O_3 strip, 80 µm wide, and intercalating hydrogen at 700 C.



Extended Data Fig. 8 | Characteristics of a SEG field effect transistor. See also SI. Sec. 4. (a) Schematic of field effect transistor with SEG as channel. (b) Transfer characteristics (I_{ds}-V_{gs}) at bias voltage of 0, 1 and 2 V. (c) Transfer curve of the device at V_{ds} = 1 V and corresponding logarithmic plot. (d) Output characteristic curves of the device. The field effect mobility is μFET = 22 $cm^2 V^{-1} s^{-1}$. The large reduction compared with the intrinsic SEC properties is caused by scattering from the dielectric and large contact Schottky barriers. (e) Extrapolation of the linear rise of the output curves correspond well with the STS measured band gap (Fig. 2e).